

Application/Control Number: 10/710,675

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1. (Currently Amended) A method of fabricating a structure, comprising:

- (a) ~~forming a polysilicon layer on~~ providing a substrate;
- (b) forming a polysilicon line ~~from said polysilicon layer~~ on-said-substrate, said polysilicon line having sidewalls;
- (c) forming an insulating sidewall layer on said sidewalls of said polysilicon line;
- (d) ~~after step (c), removing a portion of said polysilicon line and a corresponding portion of said insulating sidewall layer to form a notch in said polysilicon line~~ in a contact region of said polysilicon line; and
- (e) ~~after step (d), forming a silicide layer on said sidewall of said polysilicon line in said contact region.~~

2. (Currently Amended) The method of claim 1, step (d) further including:

simultaneously removing additional sections of said polysilicon line and corresponding sections of said insulating sidewall layer to sever said polysilicon line into gate segments.

3. (Original) The method of claim 1, wherein said polysilicon line is in the shape of a closed loop.

4. (Original) The method of claim 1, further including:

between steps (d) and (e) forming a doped silicon region in said substrate; and

said silicide layer extending over and in direct contact with at least a portion of said doped silicon region.

5. (Original) The method of claim 4, further including:

between steps (a) and (b) forming a gate dielectric on a top surface of said substrate.

6. (Original) The method of claim 1, wherein said silicide layer is selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide and platinum silicide.

7. (Currently Amended) The method of claim 1, further including:

between steps (a) and (b), forming another silicide layer on said top surface of said polysilicon line layer.

8. (Original) The method of claim 7, wherein said another silicide layer includes a material selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide and platinum silicide.

9. (Original) The method of claim 1, wherein said polysilicon line is doped N-type or P-type.

10. (Original) The method of claim 1, wherein said polysilicon line in said contact region has a width less than said polysilicon line in regions of said polysilicon line immediately adjacent to said contact region.

11. (Currently Amended) The method of claim 1, further including:

between steps (b) (g) and (e) (h) forming an insulating capping layer over a top surface of said polysilicon line; and

step (d) including simultaneously removing corresponding sections of said insulating capping layer in said contact region of said polysilicon line.

12. (Currently Amended) A method of fabricating a static random access memory (SRAM) cell; comprising:

(a) providing a substrate and forming a dielectric layer on a top surface of said substrate;

(b) forming a polysilicon line on a top surface of said dielectric layer;

(c) forming an insulating sidewall layer on said sidewalls of said polysilicon line;

(d) removing segments of said polysilicon line and corresponding portions of said insulating layer to form a first gate segment common to a first PFET and a first NFET and a second gate segment common to a second PFET and a second NFET, said first and second gate segments having top surfaces, sidewalls and ends;

(e) forming source and drains of ((a)) said first PFET, ((a)) said second PFET, ((a)) said first NFET, said second NFET, a third NFET and a fourth NFET in said substrate;

(f) forming a first silicide layer contacting a first of said ends of said first gate segment and a drain of said second PFET;

(g) forming a second silicide region contacting a contact region of at least one said sidewalls of said second gate segment and a drain of said first PFET;

(h) forming a third silicide region contacting a contact region of at least one said sidewalls of said first gate segment and a drain of said second NFET;

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(i) forming a fourth silicide region contacting a first end of said ends of said second gate segment, a drain of said first PFET and a drain of said fourth NFET; and

(j) forming a fifth silicide region contacting a second end of said ends of said first gate segment and a drain of said third NFET.

13. (Previously Presented) The method of claim 12, step (d) further including:

removing a first partial section of said polysilicon line and a corresponding portion of said insulating sidewall layer to form said contact region of at least one sidewall of said sidewalls of said first gate segment, said first partial section insufficient to completely sever said first gate segment; and

removing a second partial section of said polysilicon line and a corresponding portion of said sidewall layer to form said contact region of at least one sidewall of said sidewalls of said second gate segment, said second partial section insufficient to completely sever said second gate segment.

14. (Original) The method of claim 12,

step (c) further including: forming an insulating capping layer over said top surfaces of said first and second gate segments; and

step (d) further including: removing a corresponding portion of said insulating capping layer in said contact region of at least one sidewall of said sidewalls of said first gate segment and removing a corresponding portion of said insulating capping layer in said contact region of at least one sidewall of said sidewalls of said second gate segment.

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15. (Original) The method of claim 12, wherein:

a width of said first gate segment in said contact region of at least one said sidewall of said first gate segment is less than a width of said first gate segment in regions of said first gate segment immediately adjacent to said contact region of at least one said sidewalls of said first gate segment;

a width of said second gate segment in said contact region of at least one said sidewall of said second gate segment is less than a width of said second gate segment in regions of said second gate segment immediately adjacent to said contact region of at least one said sidewalls of said second gate segment.

16. (Previously Presented) The method of claim 12, wherein:

step (b) is performed after step (a); step (c) is performed after step (b); step (d) is performed after step (c); step (e) is performed after step (d); step (f) is performed after step (e); step (g) is performed after step (f); step (h) is performed after step (g); step (i) is performed after step (h) and step (j) is performed after step (i).

17. (Currently Amended) The method of claim 14, further including:

forming a sixth silicide region on said top surfaces of said first and second gate segments and under said insulating capping layer.

18. (Currently Amended) The method of claim 12, wherein:

step (d) includes forming a third gate segment; and

further including forming contacts to the sources of said first PFET, second PFET, first NFET, second NFET, third NFET and fourth NFET, at least one of said contacts overlapping either said first gate segment, said second gate segment or a third gate segment and overlapping one of said sources of said first PFET, second PFET, first NFET, second NFET, third NFET and fourth NFET, said at least one of said contacts in electrical contact to one of one of said sources of said first PFET, said second PFET, first NFET, second NFET, third NFET and fourth NFET but not in electrical contact with said first gate segment, said second gate segment and said third gate segment.

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